DIRECT FABRICATION OF a-Si:H THIN FILM TRANSISTOR ARRAYS ON PLASTIC AND METAL FOILS FOR FLEXIBLE DISPLAYS

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ABSTRACT

In this paper we describe solutions to address critical challenges in direct fabrication of amorphous silicon thin film transistor (TFTs) arrays for high information content active matrix flexible displays for Army applications. For all flexible substrates a manufacturable handling protocol in automated display-scale equipment is required. For metal foil substrates the principal challenges are planarization and electrical isolation, and management of coefficient of thermal expansion induced stress (CTE mismatch) during TFT fabrication. For plastic substrates the principal challenge is dimensional instability management.

1. INTRODUCTION

Flexible displays promise to usher in a new era of revolutionary and powerful anytime – anywhere information sharing. To enable this revolution, cost-effective manufacturing strategies, protocols and processes must be developed. The mission of the Flexible Display Center (FDC) at Arizona State University (Morton and Forsythe, 2007) is to dramatically accelerate the commercialization of advanced high information content flexible display technologies. This mission is realized through execution of an aggressive Strategic Plan that simultaneously evolves the technology in the dimensions of form factor, resolution, degree of flexibility, and other performance specifications, while developing the manufacturing toolsets and processes to fabricate high quality, high technology readiness level technology demonstrators.

The Center was formed through a cooperative agreement with the Army Research Laboratory that enables the university, government and strategic industrial partners (SEE Figure 1) to work together to achieve a common goal. The initial five-year phase of this 10-year program represents a $44 million investment by the Army and a comparable commitment by Arizona State University. Industrial partners co-invest financially in the Center to support development projects at the Center, and work directly with the Center and its partners to collectively advance flexible display and associated manufacturing technology. The industrial participation is governed by a unique partnership agreement that spells out the co-investment requirements, membership benefits, and intellectual property (IP) rights of the participating organizations. The IP framework is designed to incentivize and reward participation, while protecting the commercialization rights of the Center members who bring their unique technology to the table.

Fig. 1 FDC Strategic Government-University-Industry Partnership

This paper describes critical challenges in flexible display manufacturing and associated FDC strategies and solutions. In the context of accelerating flexible display commercialization, we are seeking solutions that create a robust flexible display manufacturing supply chain and that can readily and effectively leverage the tremendous historical investment in amorphous silicon (a-Si:H) thin film transistor (TFT) manufacturing infrastructure for commercial glass-based flat panel displays.

2. CRITICAL MANUFACTURING CHALLENGES

At a high level the critical manufacturing challenges for active matrix flexible displays are summarized in Figure 2 at the top of the following page.

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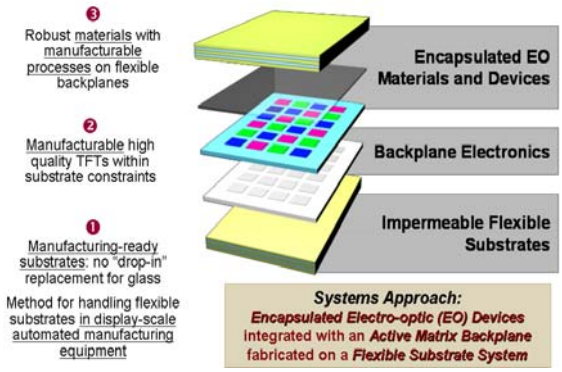

Fig. 2 Summary of Critical Manufacturing Challenges for Flexible Displays

These challenges can be categorized by the three principal subsystems comprising a flexible display: (i) impermeable flexible substrate systems "display-ready" materials and handling protocols, (ii) high performance TFT devices and circuits fabricated for backplane electronics within the constraints of the flexible substrate systems, and (iii) robust electro-optic frontplane materials, devices and processes for integration with the flexible TFT arrays. Approaches and solution to address each of these major challenges are described in the following section.

3. EXPERIMENTAL APPROACH AND RESULTS

Manufacturing Pilot Line Development Flexible display and associated manufacturing technology development described in this paper was conducted on the Center's 150 mm wafer-scale Pilot Line as described in detail elsewhere (Raupp *et al*., 2007). Note that Pilot Line scale-up to GEN II display-scale (370 x 470 mm) is complete and underway transition of processes is well enderway. The 6" line is operated by a dedicated full-time permanent professional staff, and is linked to a *MassGroup* Manufacturing Execution System (MES) that provides a high level of real time integrated information on Lot status and operational capability, and facilitates yield enhancement and troubleshooting.

Fully automated E-test is provided by an FDC custom hardware integration of Electroglas probers with Keithley electronics. Two probers run continuously (24/7) under FDC-custom LabView control to provide detailed I-V characteristic curves for a representative set of TFTs on each substrate, and an additional prober is employed to provide TFT array test for uniformity and yield. A forth prober provides automated array repair for disply builds. Cycle time for TFT array fabrication and E-test is 2-3 weeks, thereby allowing many cycles of process improvement aimed at rapidly providing higher performance TFTs at higher yield.

Flexible Substrate Handling Protocol To enable high quality TFT arrays to be directly fabricated on flexible substrates in automated manufacturing tools that are built to process rigid glass substrates, the FDC developed a temporary bonding / de-bonding approach (Raupp *et al*., 2007). In this handling protocol a flexible substrate is temporarily adhered to a rigid carrier plate with a releasable adhesive, and the carrier-adhesive-substrate system is then processed using standard automated TFT fabrication tools. The rigid carrier gives the structural support required by the handlers and the process tools and suppresses deformation of the flexible substrate during processing. Following full TFT array fabrication the flexible substrate is released from the carrier through any of a number of triggered release mechanisms including mechanical, solvent, ultraviolet light or thermal release processes.

Alternative handling and fabrication approaches developed elsewhere include a coat – laser release process and a layer transfer process. In the coat – laser release process a thin polymer layer is cast from solution (typically polyimide spin-coating), followed by microelectronics fabrication and backside excimer laser-induced release by melting/ablation of the polyimide at the glass-polymer interface (Arjavalingam *et al.* 1993; Doany and Narayan, 1997). Philips has developed a version of this process known as EPLaR™ (electronics on plastic by laser release) to produce TFT arrays for reflective flexible displays (French and McCulloch, 2005; Lifka *et al*., 2007). In the layer transfer process, TFT arrays are fabricated directly on glass and then laser-released and transferred to a flexible substrate. Seiko-Epson has pioneered this approach to produce poly-silicon TFT arrays with a process they have trademarked as SUFTLA™ (Surface Free Technology by Laser Annealing/Ablation) (Hashimoto *et al*., 2006; Miyasaka, 2007). Each of the three processes has unique inherent advantages and limitations, and all are likely to move forward to flexible electronics and flexible display manufacturing in the near future.

The FDC temporary bonding protocol required simultaneous development of new custom carriers and temporary adhesive materials, adapted manufacturing toolsets for automated bonding and debonding, and development of new robust processes and handling protocols. A key to successful demonstration of this technology was a systems-level methodology that considered the fundamental thermo-mechanical interactions of the substrate carrier – adhesive – substrate – planarization layer system. A second key was the development of custom high performance temporary adhesives tailored for our substrates and process temperatures (SEE next sections) by *National Starch* through a *Flextech Alliance*-funded program.

The most significant issue encountered with this approach is the stress that is developed during the bonding-debonding processes as well as during the TFT direct fabrication process steps. These steps typically employ high temperature processing, which exacerbate the thermal property mismatches between the carrier,

adhesive, and flexible substrate. These thermal property mismatches lead to bowing (changes in radius of curvature) of the carrier system during thermal processing and this bowing can lead to wafer handling problems in processing equipment or delamination of the flexible substrate from the rigid carrier. In our work different carriers, flexible substrates, and adhesives were evaluated to study the thermal mismatches and subsequent bowing of various systems. Our proprietary carrier showed a significant decrease in bonded system bow as compared to systems bonded with a conventional silicon carrier. These lower bow values were a result of a lower coefficient of thermal expansion (CTE) mismatch between our carrier and various substrates as compared to silicon. In addition to a lower CTE mismatch with our carrier, the bow of systems bonded to our carrier was further reduced due to a higher Young's modulus as compared to silicon.

Properties of the adhesives used to bond the flexible substrate to the rigid carrier were found to have a significant affect on the bow of the bonded system. Adhesives with increased content of high molecular weight polymer were found to give a greater increase in the bow of the system. For cross-linkable adhesive systems, the effect of crosslink density was investigated on the bow of the wafer. In summary the properties of the rigid carrier, flexible substrate, and adhesive must all be considered in the selection of a bonded flexible substrate system.

Flexible Substrates and Issues Candidate flexible substrates that could be employed in a bond-debond handling protocol include a number of plastic films and metal (primarily stainless steel) foils. Principal issues to be addressed with direct fabrication on stainless steel (SS) substrates were surface roughness and CTE management in process. To minimize the CTE issues we selected a low CTE Type 430 SS substrate as our preferred SS substrate. For SS roughness we sought a planarization solution over a polishing solution, since we deemed polishing to be too high cost from a manufacturing perspective. For planarization and electrical passivation, a new spin-on "planar thermally-stable" (PTS) thin film material from FDC partner *Honeywell Electronic Materials (HEM)* was employed. Based on AFM analysis, the planarization layer was capable of reducing root-mean-square roughness from 24.5 nm as received to 2.9 nm, and the peak-to-valley roughness from 230 nm to 20 nm. With a 100 μm thick low CTE SS substrate and a 2.0 μm HEM planarization layer, greater than 99.98% TFT yield over a 320x240 3.8-in. diagonal TFT array can be achieved. The most severe defects are shorts to the substrate, indicating a need to continue to further improve the base material and the planarization layer and process for a fully-manufacturable material and process.

For plastic substrates the two principal issues to be addressed were dimensional stability, in this case run-out, due to induced stress from deposited films, and surface roughness. In the context of these intrinsic plastic materials limitations, the FDC selected heat-stabilized PEN (HS-PEN) from member company *DuPont Teijin Films* (*DTF*) as the preferred low temperature transparent polymer substrate because of its relatively good dimensional stability and good surface properties. This selection limited the maximum a-Si:H TFT fabrication process temperature to 180 °C.

We worked with DTF to screen a number of planarization layer candidates and down-selected to the preferred option; DTF now provides their PEN in a form with an integrated planarization layer (known as *Planarised PEN*™), which is now the FDC-preferred plastic substrate. Through a combination of process modifications implemented by the FDC, careful design of the custom temporary adhesive, and materials improvements achieved by DTF, we were able to reduce the maximum distortion to essentially a negligible value (less than 10 ppm) for all process steps. This distortion level readily enables good layer registration over a 3.8-in. diagonal TFT array (105 ppi) and greater than 99.9% functional TFT yield within the array.

TFT Fabrication and Performance Inverted staggered trilayer a-Si:H TFTs were employed in this work (Raupp *et al*., 2007; O'Rourke *et al*., 2008a). The maximum process temperature was 180 °C, which occurred during plasma enhanced chemical vapor deposition (PECVD) of the silicon nitride gate dielectric, a-Si:H semiconductor channel, and n^+ a-Si:H contact layers. In the fabrication sequence a 300 nm silicon nitride (SiN:H) passivation layer was first deposited by PECVD, and a molybdenum film was then deposited by DC sputtering for gate bus lines. A 300 nm thick SiN:H film, an 80 nm a-Si:H film and a 100 nm SiN:H film were deposited consecutively by PECVD. Following formation of a-Si:H islands, a 100 nm thick SiN:H layer was deposited to passivate the a-Si:H sidewall, and vias to the backside of the a-Si channel were wet etched. The data lines and contacts were formed by PECVD deposition and patterning of n^+ doped a-Si:H and Al metal by DC sputtering. Finally, a 2 μm thick PTS-R dielectric was spin-coated, followed by Mo and ITO sputter deposition and photolithographic patterning to form the passivation and pixel electrode, respectively. Figure 3 is a photograph of a portion of a typical transistor array on SS.

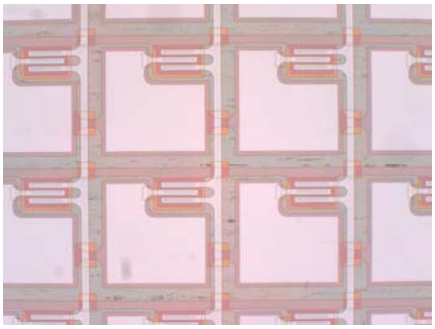

Fig. 3. Optical Micrograph of TFT Array Pixels on a Planarized SS Substrate

The FDC baseline pilot line fabrication process produces bottom-gate channel-passivated TFTs with statistically-averaged saturation mobility μ_{sat} of 0.7 cm^2/V-s, ON/OFF Ratio (20 Vds, -15 Vgs) of nearly 10^9, sub-threshold slope of less than 0.5 V/decade, and threshold voltage of 1.6 V. Figure 4 shows typical TFT output and transfer characteristic curves. A mild hysteresis on the order of 0.3 V is evident in the transfer curves, which is reflective of the low processing temperatures. Except for this hysteresis and threshold voltage shift characteristic of low temperature a-Si:H TFTs, these metrics compare quite favorably with those exhibited by commercial a-Si:H TFTs fabricated on glass at much higher temperatures (Shin, 2007). Note that these performance values are average results quoted for automated testing of 16 test transistors with a 96 μm channel width W and 9 μm channel length L (W/L = 10.67) on each of twelve substrates in a lot, and for multiple lots. Fit yields for these process control monitoring (PCM) structures are typically 100%, and these performance metrics are essentially indistinguishable between lots run with flexible SS or PEN or rigid silicon or glass substrates.

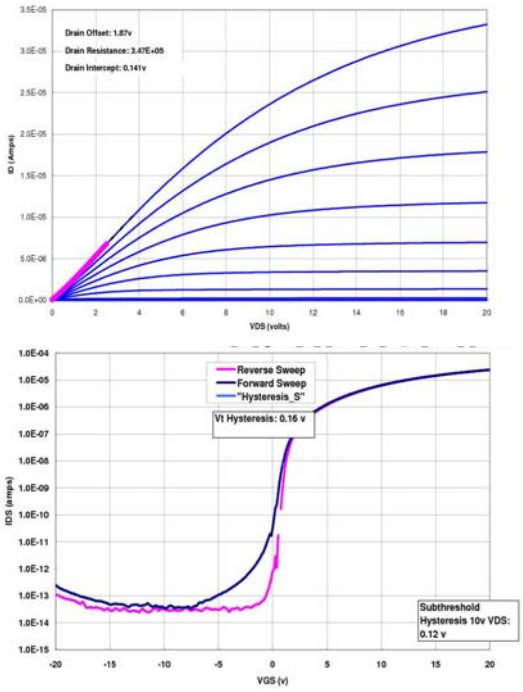

Fig. 4. Typical performance characteristics of a-Si TFTs fabricated on planarized stainless steel: (a) output characteristics; (b) transfer curves

4. DISPLAY TECHNOLOGY DEMONSTRATORS

Figure 5 shows photographs of 3.8-in. QVGA electrophoretic ink displays (EPDs) fabricated on both low CTE SS and HS-PEN. Both displays have a small number of line defects, but exhibit good contrast ratio and grey-scale (4-bit) and fast image switching speed (~0.35 s). We continue to improve our processes and protocols in an effort to produce even higher quality displays. Through a focused defect reduction program we have recently been able to produce zero-line-defect panels on SS. We are now embarking on a major defectivity reduction program with the plastic substrate.

Fig. 5. 3.8-in diagonal QVGA EPD panels on SS (top) and on HS-PEN (bottom). The displays were produced with FDC partner *E Ink's* Vizplex 100™ imaging film integrated at the FDC.

5. CONCLUSIONS

This work demonstrates that a viable and effective pathway exists for direct fabrication of high quality flexible reflective displays on two candidate flexible substrate types in a Pilot Line manufacturing environment. We are now transitioning this technology know-how to our GEN II (370 x 470 mm) Pilot Line to demonstrate scalability and manufacturability on display-scale equipment, which will be a crucial milestone towards transitioning FDC know-how and processes to a flexible display commercial manufacturer.

Two rapid technology transition modes are "built in" to the partnership to realize the commercialization acceleration objective. In the first mode, manufacturing supply-chain partners commercialize

enabling materials and new manufacturing tools developed through the FDC partnership through their marketing and sales arms. This paper described two such enabling materials commercialization successes already realized; additional successes in manufacturing tool hardware and software have likewise been realized (although they were not described here).

In the second technology transition mode (O'Rourke *et al*., 2008b), Army system integrator partners such as *General Dynamics C4S, Raytheon* and *Boeing* take flexible display panels produced by the FDC and integrate them into fully functional product-level demonstrators, which are then in turn delivered to the U.S. Army or the company's own internal customers for evaluation. These demonstrators highlight the compelling advantages of flexible display technology for the Warfighter, and allow PEOs and PMs the opportunity to evaluate this revolutionary technology and anticipate their insertion in future systems.

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